

Fig. 1

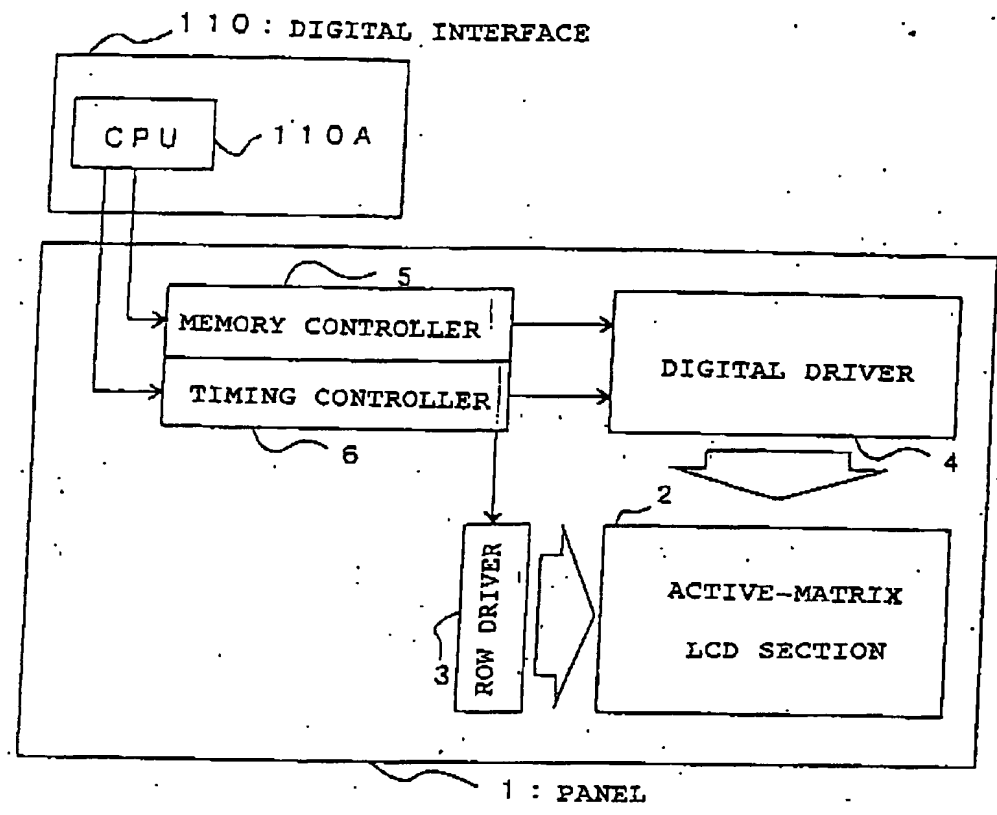


Fig. 2

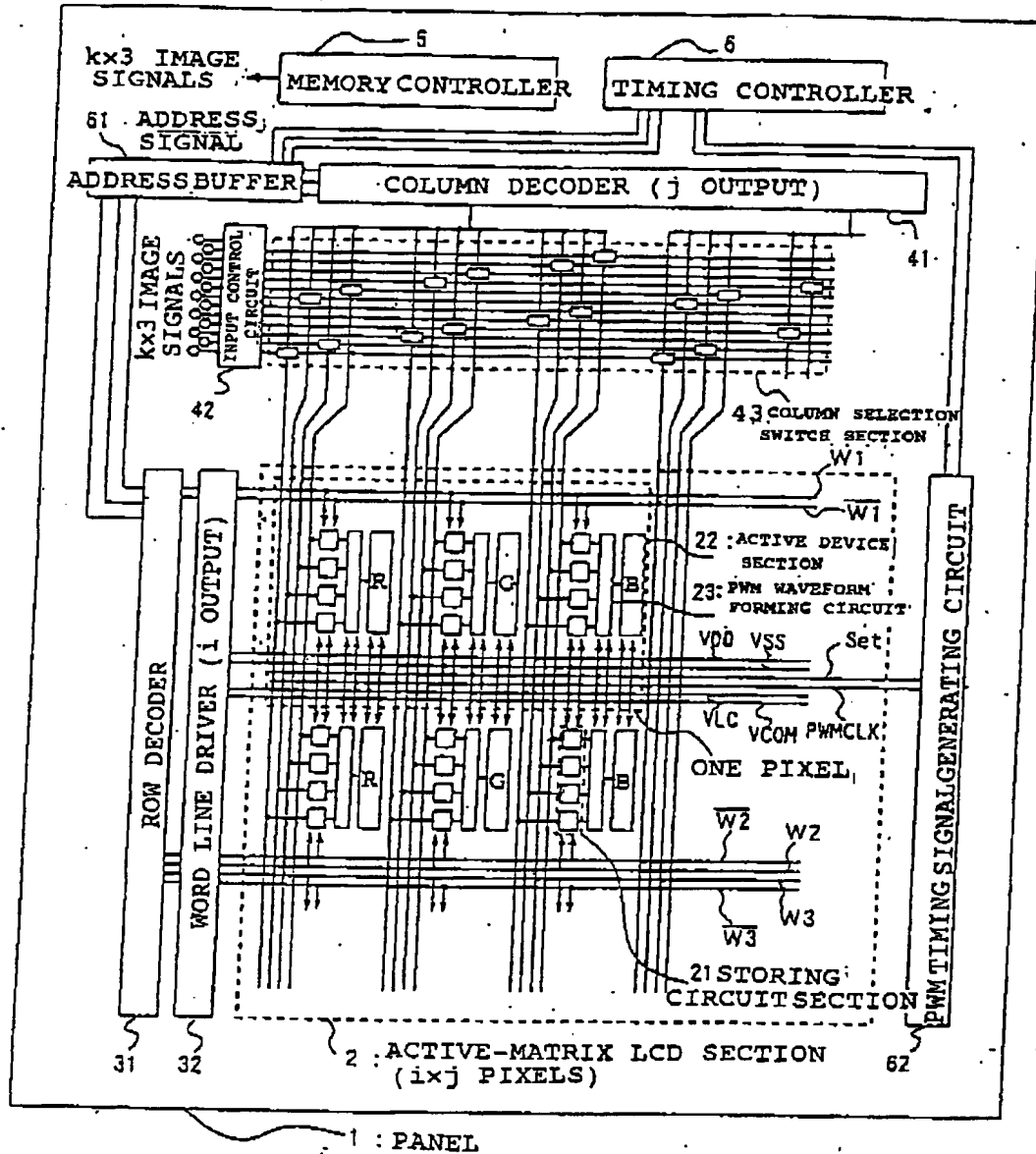


Fig. 3

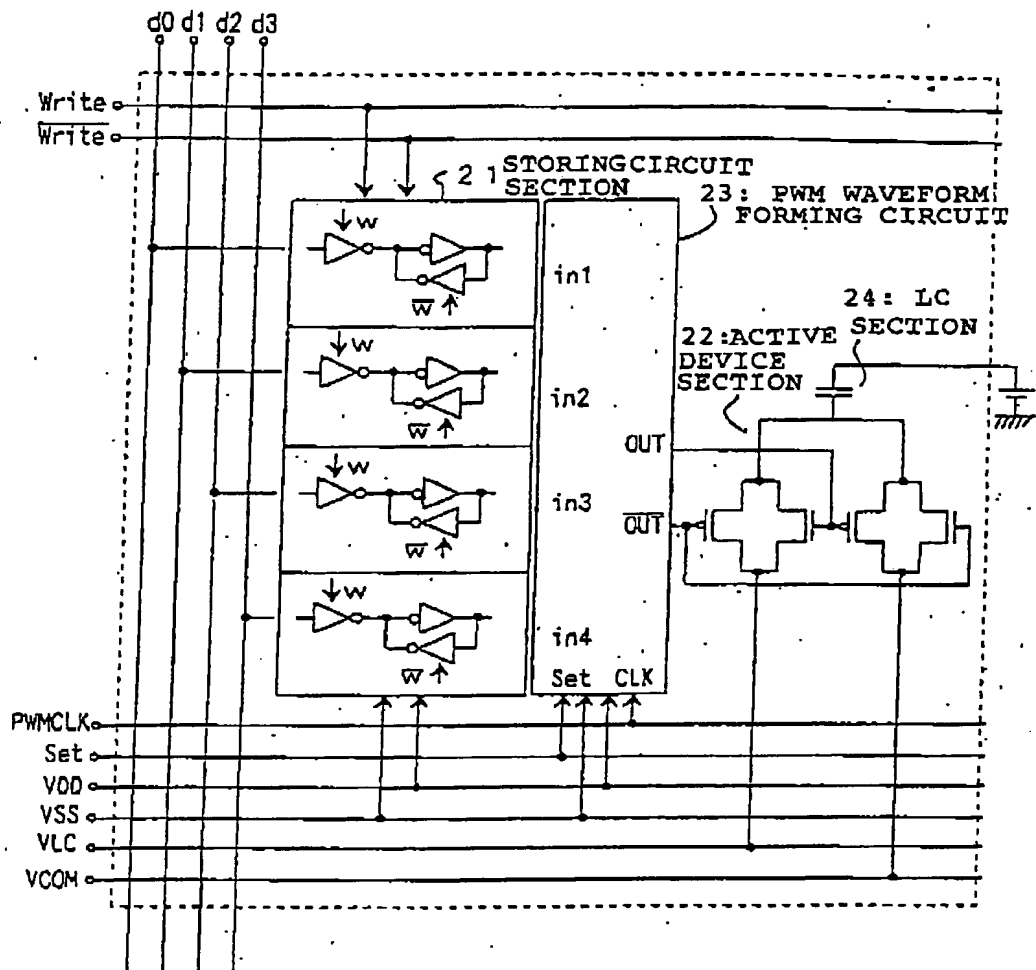
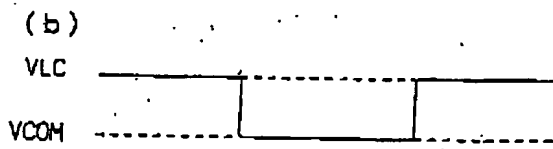
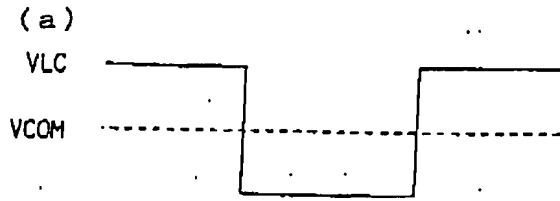


Fig. 4



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Fig. 5

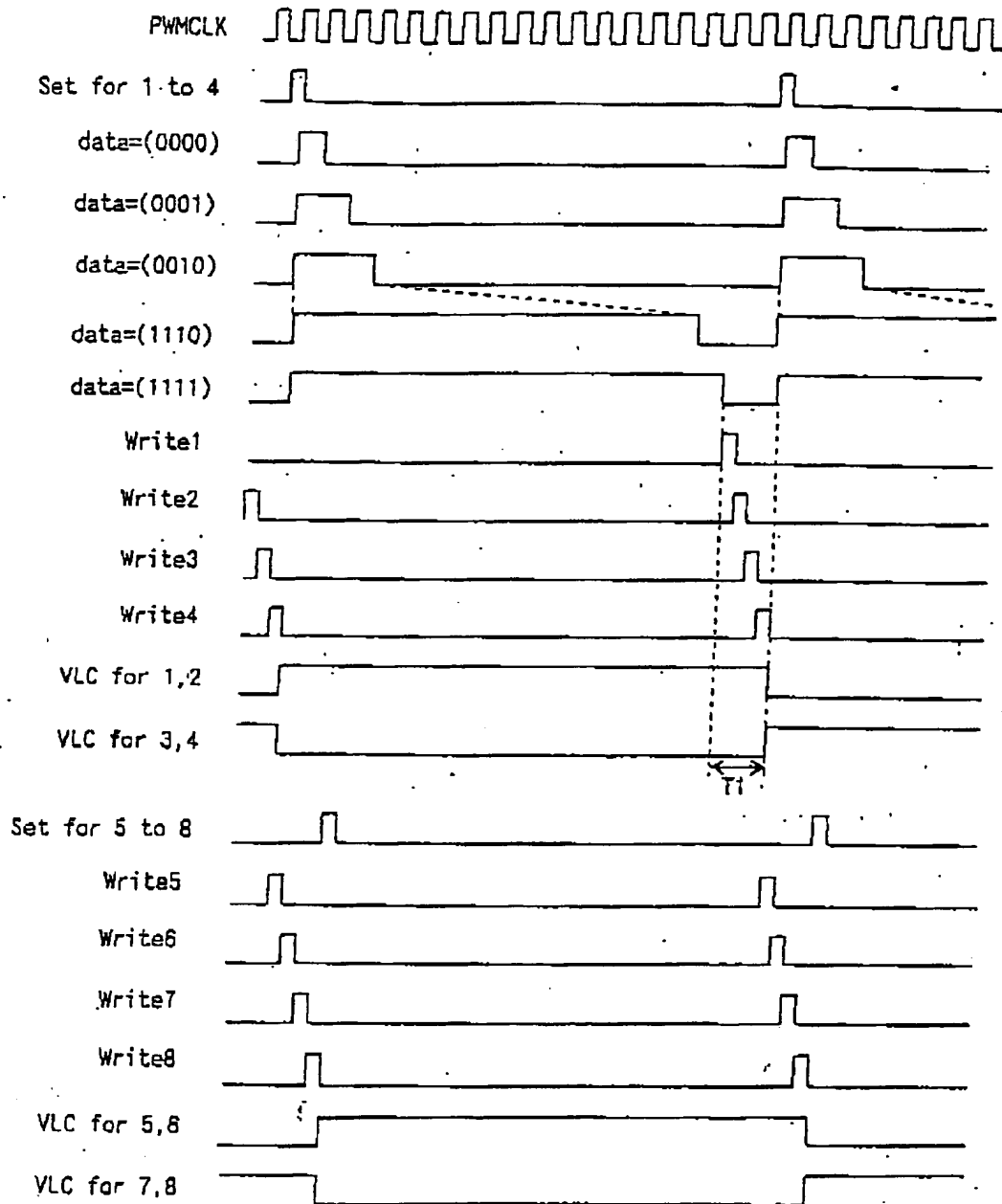


Fig. 6

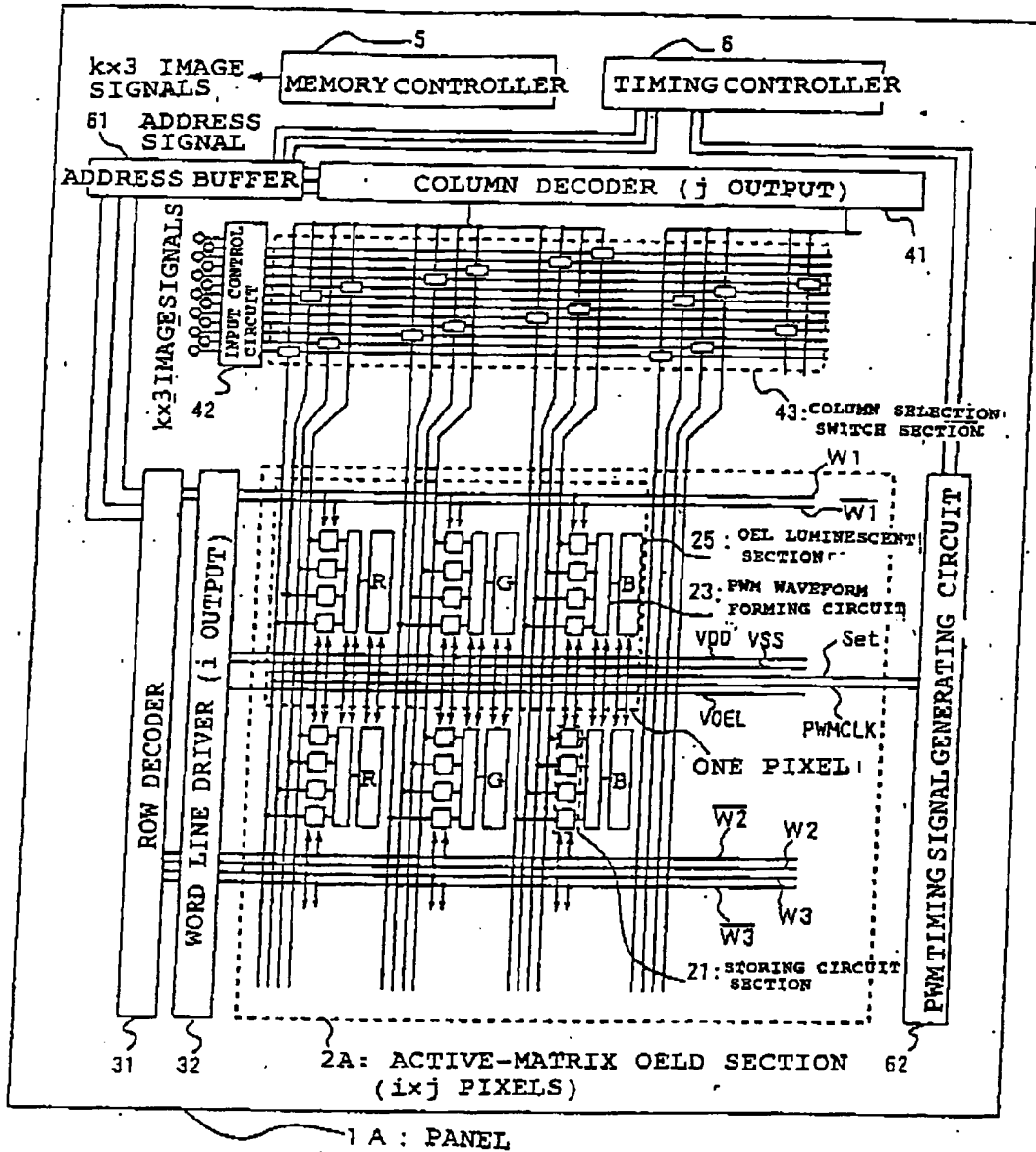


Fig. 7

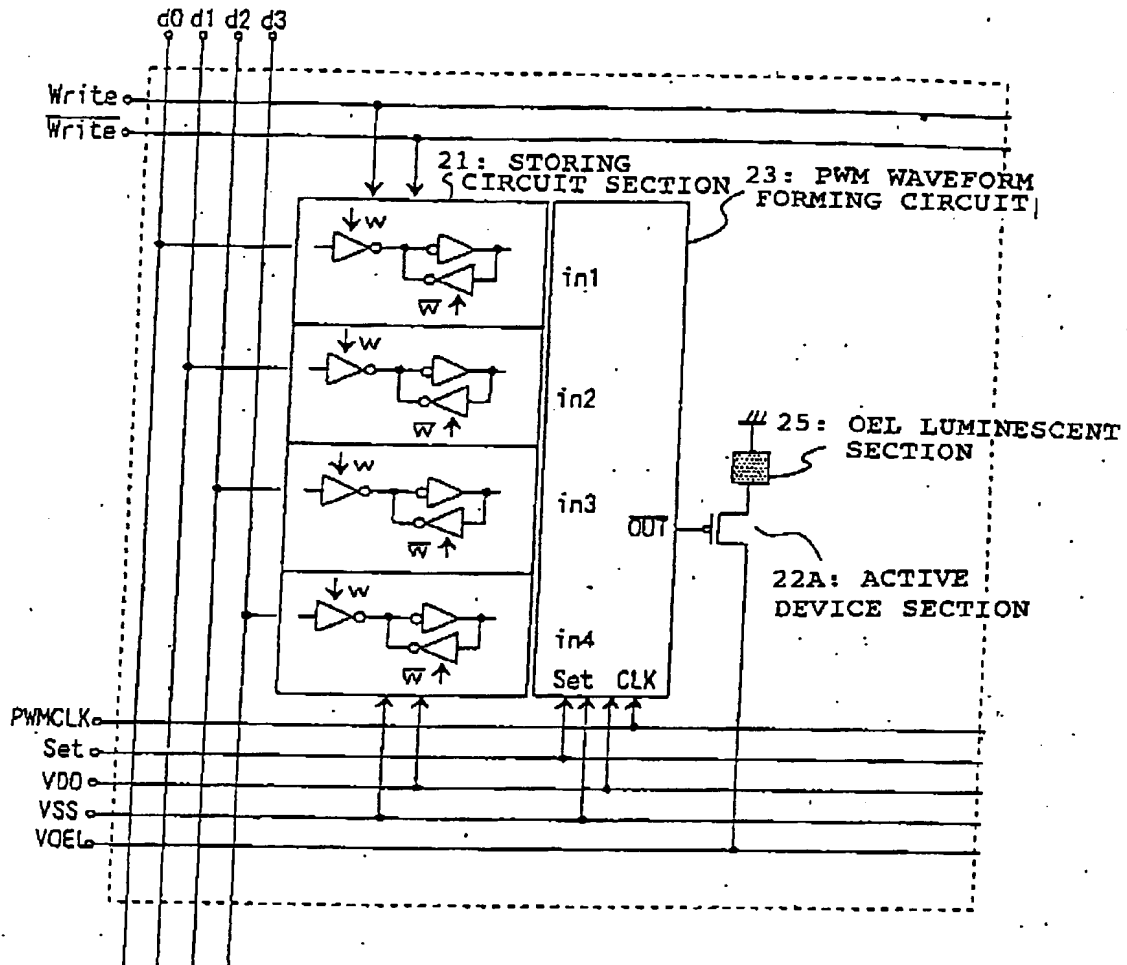


Fig. 8

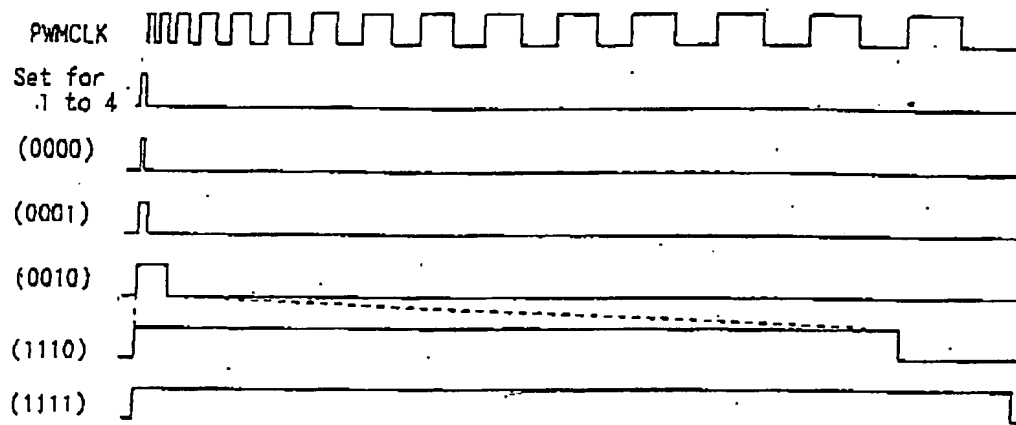


Fig. 9

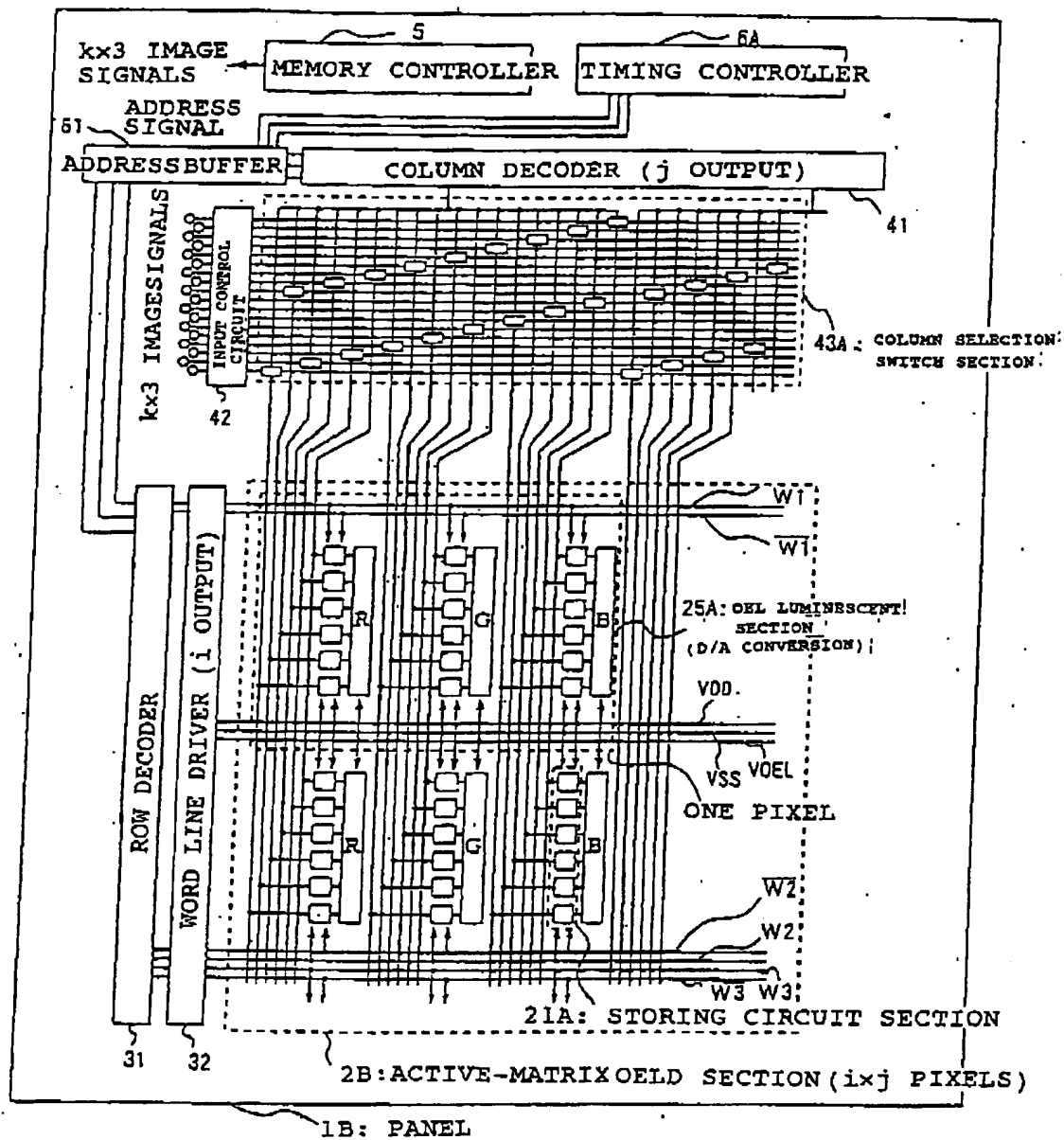
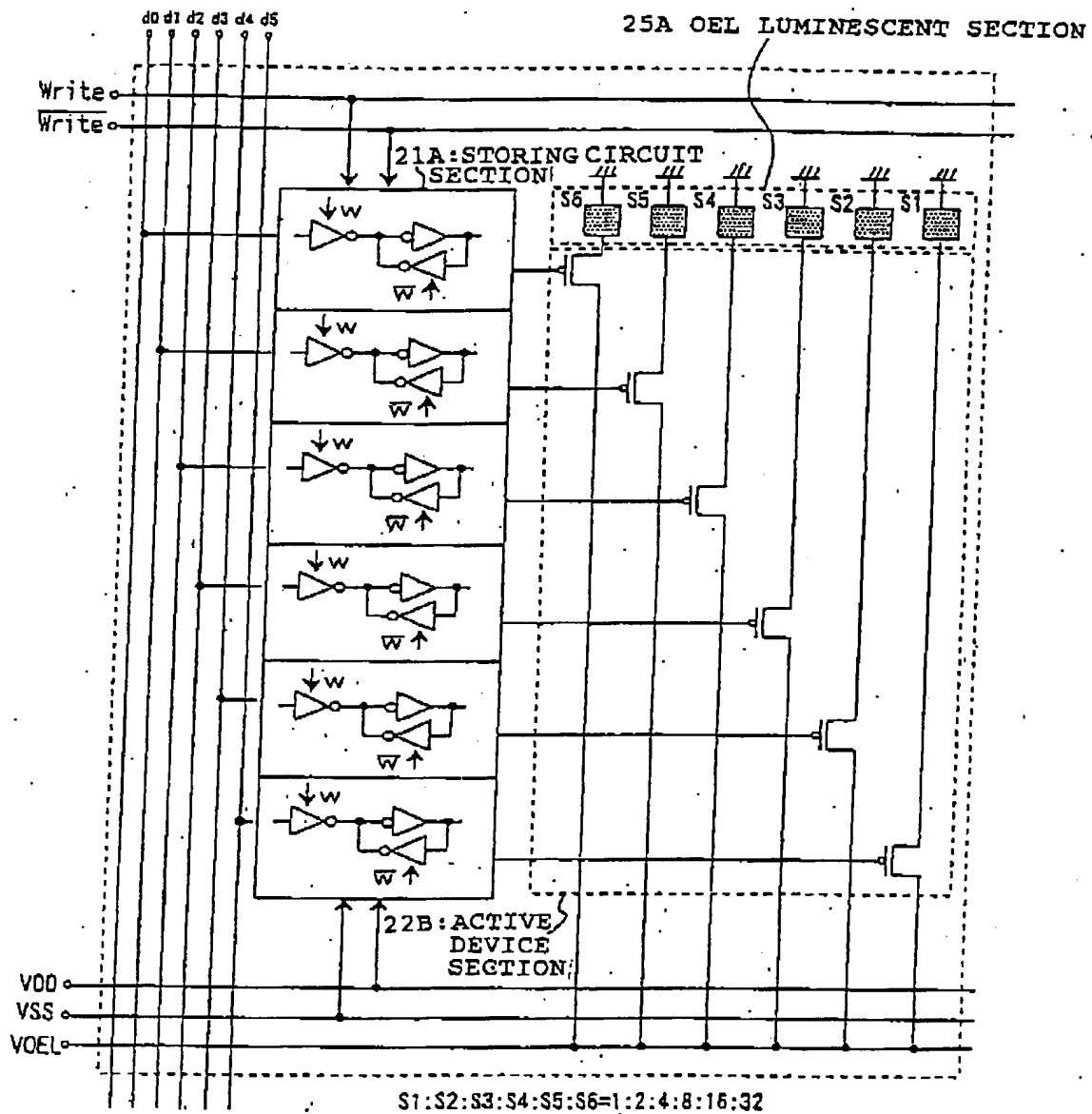


Fig. 10



1C: PANEL

2C: ACTIVE-MATRIX LCD SECTION ($i \times j$ PIXELS)

31 ROW DECODER

32 WORD LINE DRIVER (i OUTPUT)

42 INPUT CONTROL CIRCUIT

438: COLUMN SELECTION SWITCH SECTION

22: ACTIVE DEVICE SECTION

21: STORING CIRCUIT SECTION

ONE PIXEL

V00 VSS

VLCON VLCOFF (VCOM)

W1 W2 W3

W1 W2 W3

5 MEMORY CONTROLLER

5A TIMING CONTROLLER

61 ADDRESS SIGNAL

ADDRESS BUFFER

COLUMN DECODER (j OUTPUT)

kx3 IMAGE SIGNALS

Fig. 12

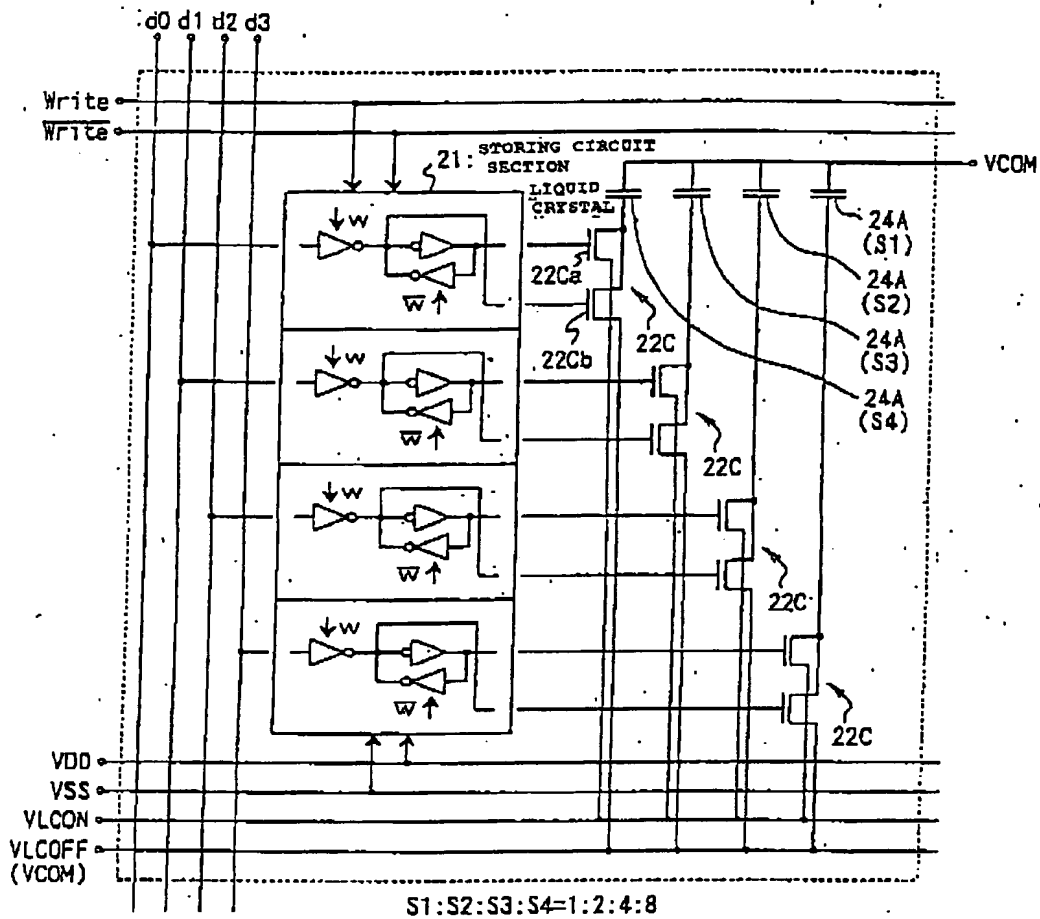


Fig. 13

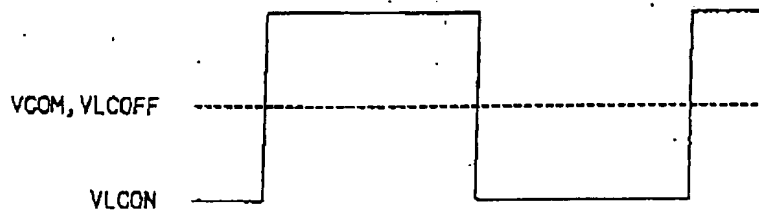


Fig. 14

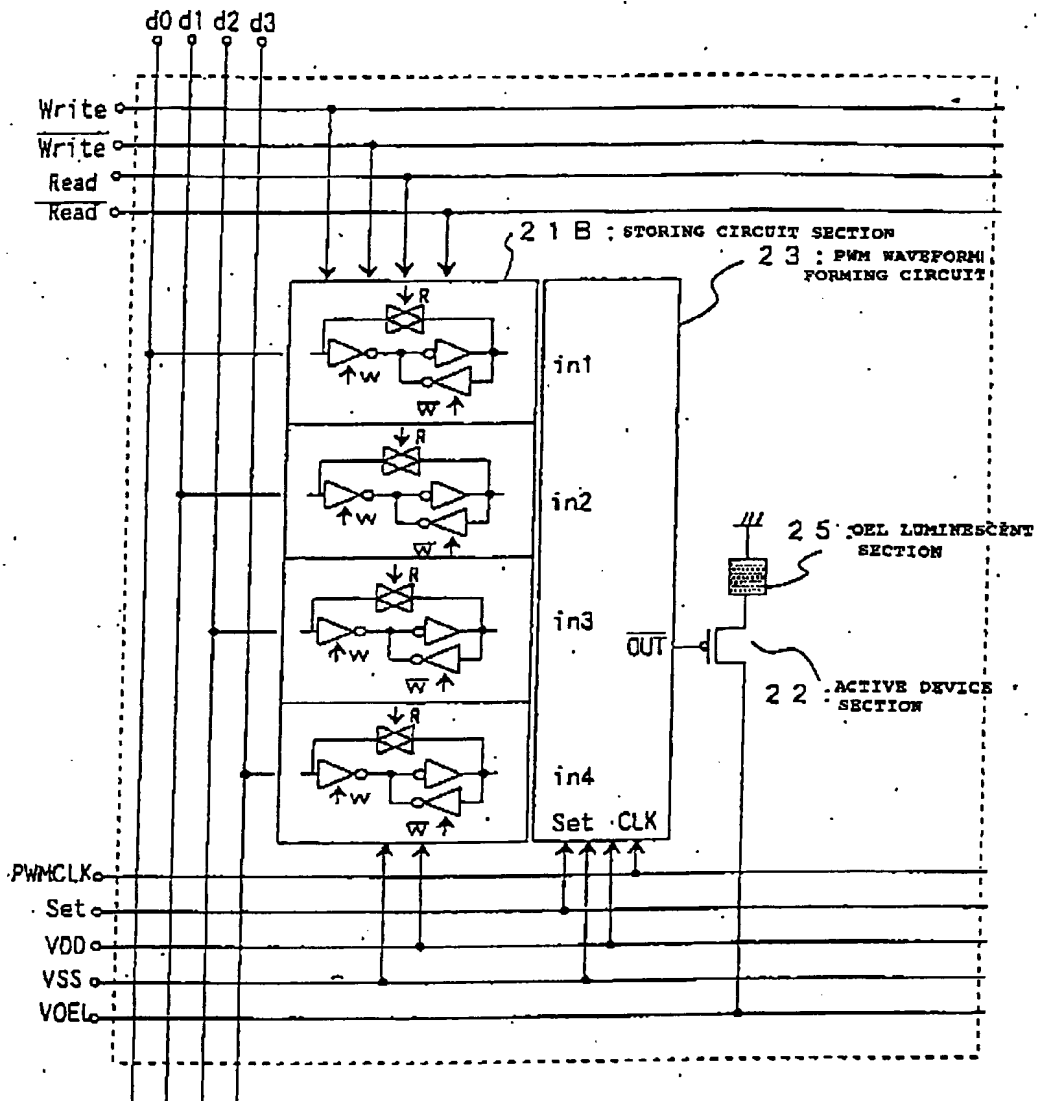


Fig. 15

